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Sommario	The aim of this project is the design and the realization of a 30 kV reference voltage divider (VD) for smart grid monitoring, which will be mainly used in laboratories to characterize and calibrate the voltage transducers. The scale factor ratio error introduced by a normal voltage transducer (VT), according to technical report IEC/TR 61869-103 must be limited to a maximum of 1% up to 2nd harmonics and to a maximum of 5% up to the 50th harmonics. The maximum acceptable phase error should be no more than 18 mrad up to the 2nd harmonics and 90 mrad up to the 50th harmonics. Of course, the target for a reference voltage transducer should be much more accurate than the requirement of the standards for a normal VT. A reference voltage transducer is expected to show high accuracy also at higher frequencies, since this feature is needed in smart grids, due to the considerable amount of harmonics after the 50th harmonics even up to 10 kHz, although this peculiarity is not required by the standards for transducers in normal electrical networks. Then, in the bandwidth up to 10 kHz, the maximum target deviation from the rated scale factor for the reference VD has been selected equal to 0.05 % and the maximum phase error equal to 9 mrad. To reach such a high accuracy, there is a need for a design tool, which can model and simulate the divider with a very good

accuracy. Then, this tool could be used for the design procedure of the structure and of the definition of the geometrical parameters of the reference VD, in order to realize an extremely accurate measurement device satisfying the demanding constraints mentioned above. To begin with, two methods, the Finite Element Method (FEM) and the Boundary Element Method (BEM), were examined in calculating the stray capacitance between two (physically infinite) planes. The comparison of BEM and FEM results with the analytical ones shows a better accuracy and a lower CPU simulation time in FEM rather than in BEM approach. Thus, the physical model of the reference VD has been simulated by FEM. The output of the FEM software is a matrix defining the stray capacitance network between different nodes (equipotential surfaces) of a voltage divider. This matrix is used as an input of a MATLAB program, which solves the electrical circuit of the VD. Furthermore, a small voltage divider was realized to prove the capability of this modeling approach. The measurement results of the test VD shows a good agreement with the results obtained from the theoretical method. An innovative approach was presented in the modeling of resistors, which have been divided into two parts, instead of being modeled as a single component. The important role of the resistor body modeling in calculating the stray capacitances in the VD has been highlighted. The validation procedure was repeated for a real 20 kV VD that was already available. The comparison between measurement and theoretical results confirms the validity and high accuracy of the proposed modelling approach. The research carried out up to here has been published in "IEEE Transaction on power delivery". The realization of the numerical tool has allowed the design of the reference 30 kV VD. The first issue was to find the best configuration for the VD. It is not clear in literature what kind of configuration could be the best or what should be considered in the design and realization course. Such a lack of guidelines is the main reason that impeded the application of an optimization method in this project. In fact, the optimization process could be used for a device, which has a known and fixed configuration with a limited number of geometrical and electrical variables that can be selected in order to find the best value for the best objective function. The design realized in this project aimed also at configuring shape and structure of the divider for future optimization process. In other words, some different VD configurations and effect of different parameters variation have been deeply investigated. At the start of assessment, different kind of stray capacitances and their effect on the frequency behavior of a VD have been discussed. This subject has been investigated by introducing the equivalent circuit of a simple VD. Then the effect of modifying different kind of stray capacitances on the VD frequency behavior has been shown. Besides, the best condition for the stray capacitances that can lead to a good frequency behavior has been discussed. The initial VD design procedure was done in order to mainly understand the effect of geometrical parameters like the distances between the HV resistors and between HV and LV sections. The goal was to lower (and also balance) the stray capacitances. Then, a grounded plate has been introduced and discussed in the resistive VD with horizontally placed resistors, in the attempt of reducing and better balancing the stray capacitances. The effect of the presence and also the size of the plate has been discussed and the effect of the distances between the resistors were also studied (Section 3.3). At this stage, new circuital components have been introduced in the

divider. The compensation of the low voltage (LV) side with an extra LV capacitor (CBT) is explained (this subject is explained in detail in section 3.3.7). As the next step, a Reference Voltage Divider (RVD) considering the voltage requirements (30kV) and high voltage (HV) resistors (with rated voltage of 10 kV) has been designed. The first design has been dedicated to the simplest configuration with vertically placed HV resistors. Then the geometrical parameters (distances) has been changed and the effect was studied. At the end of this part, a VD configuration with vertically placed HV resistors has been modelled and simulated. The simulation has been carried out with an accurate model including all the details of the components available for the VD realization like, for instance, insulation supports, resistors and pillars. Design simulations show very good results that comply the uncertainty limitations of a reference VD. However, there was a drawback in that first design configuration. Its size was quite large compared to the similar measurement devices in this voltage range. Despite this fact, the finalized RVD was realized and its frequency behavior was measured using two digitizers at the low voltage side. Although the measurement results were following the frequency behavior of the simulation results, a significant discrepancy between the measured and simulated frequency responses has been found. Section 3.6.1 show the analysis of the discrepancies between the model and measurements. The reason was due to the ground below the VD that was disregarded in the simulations. The agreement between computed and measured response of the VD with vertically placed resistors significantly improves when the ground is correctly modeled. However, the ground presence worsens the frequency behavior of the VD, which becomes undesirable for a RVD, even if acceptable with respect to the requirement of the standards for a normal voltage transducer. The analysis of the VD with vertically placed HV resistors has been published in the journal of "International review on electrical engineering". In a next step, the general behavior of the 30 kV VD with horizontally placed HV resistors has been investigated since this configuration results to be more compact and should be less sensitive to proximity objects. In the previous configuration (the vertical one), the distances between high voltage nodes were large enough that small changes in the resistor placement or in the shield dimensions do not modify significantly the electric field. However, in this new configuration (the horizontal one), the electric field must be calculated by FEM for any modification of the parameters. Two different way of connections between HV resistors were modeled (section 3.7) with long and short connections. The comparison between the two configurations shows that the VD with shorter copper tube connection have a better behavior and so has been further investigated in the following. The RVD with horizontally placed resistors could give a good frequency behavior. However, the maximum electrical field strength could not be further lowered due to the nature of this configuration (section 3.7). In order to get an improved frequency behavior a zig-zag configuration has been introduced a topological variation of the horizontal configuration. The zig-zag VD lowers the maximum electrical field strength compared to the horizontal resistor VD (section 3.8). More than 50 cases of zig-zag VD with different parameters were simulated to reach the goal of the project design. A main part of the focus was on the shielding of the RVD in a way to control and manipulate the stray capacitances in order to make the VD error compliant with the design specification. The main drawback of this zig-zag RVD is the sensitivity towards the

	proximity effect. In section 3.8.8, a shielding with three different screen parts has been proposed. Such a shield could give a good frequency behavior with small proximity sensitivity. However, the model with three screens could not be realized at the moment as it requires special workshop tools, not available at the moment. A different approach has been achieved providing a reduction of the proximity effect (section 3.10). The zig-zag RVD has been fitted with an LV shield. The measurement results show an accuracy of ±980 ppm for the scale factor, up to 50 kHz, and less than 9 mrad for the phase error up to 32 kHz (2.1 mrad up to 10 kHz). This zig-zag RVD could be used in any laboratory environment after calibration for the specified perimeter. To further reduce the proximity sensitivity, HV capacitors have been added to the zig-zag RVD, which significantly reduces the effect of the stray parameters and the VD is much less affected by the proximity changes (stray capac
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